WHAT IS CLAIMED IS:

1. A method for performing an erase operation in a non-volatile memory device comprising a bulk region of a first conductive type, spaced first and second impurity diffusion regions of a second conductive type formed in the bulk region, a charge storing layer formed between the first and the second impurity diffusion regions, and a conductive electrode formed on the charge storing layer, the method comprising the steps of:

applying a bulk voltage to the bulk region for a predetermined erase time;

applying a gate voltage to the conductive electrode for the predetermined erase time, the gate voltage being greater than or equal to the bulk voltage;

applying a first electrical signal to the first impurity diffusion region for the predetermined erase time, the first electrical signal comprising a voltage that is greater than the gate voltage; and

applying a second electrical signal to the second impurity diffusion region for the predetermined erase time, the second electrical signal comprising a voltage that is greater than the gate voltage,

wherein the voltage of the first electrical signal is different from the voltage of the second electrical signal.

2. The method of claim 1, wherein data is stored in the charge storing layer through a tunnel oxide layer, a charge storing nitride layer, and a blocking oxide layer stacked in sequence.

3. The method of claim 1, wherein the first conductive type is P-type, and the second conductive type is N-type.

4. The method of claim 1, wherein the bulk voltage is about 0V.

5. The method of claim 1, wherein the voltage of the first electrical signal is switched between a first voltage and a second voltage at least one time, during the predetermined erase time, wherein the first and second voltages are greater than the gate voltage.

6. The method of claim 5, wherein the second electrical signal is substantially equal to the first and second voltages when the first electrical signal is substantially equal to the second and the first voltages, respectively, for the predetermined erase time.

7. The method of claim 6, wherein the first voltage ranges from about 2V to about 6V, and the second voltage is about 10V.

8. The method of claim 6, wherein both the gate voltage and the bulk voltage are about 0V.

9. A method for performing an erase operation in a memory cell comprising a bulk region of a first conductive type, spaced source and drain regions of a

second conductive type formed in the bulk region, and a gate electrode formed between the source and drain regions, the method comprising the steps of:

applying a first voltage to the source region and a second voltage to the drain region for a portion of a predetermined erase time; and

applying the second voltage to the source region and the first voltage to the drain region for a portion of the predetermined erase time.

10. The method of claim 9, wherein the first conductive type is P-type, and the second conductive type is N-type, and wherein a bulk voltage applied to the bulk region is about 0V, and a gate voltage applied to the gate electrode is greater than or equal to the bulk voltage.

11. The method of claim 10, wherein the first and the second voltages are greater than the gate voltage.

12. The method of claim 9, wherein the first voltage is in the range of about 2V to about 6V and the second voltage is about 10V

13. The method of claim 9, wherein the second voltage is in the range of about 2V to about 6V and the first voltage is about 10V.

14. A method for performing an erase operation in a non-volatile memory device comprising a bulk region of a first conductive type, spaced source and drain

regions of a second conductive type formed in the bulk region, and a gate electrode formed between the source and drain regions, the method comprising the steps of:

applying a first voltage and a second voltage to the source and drain regions, respectively, for a predetermined erase time;

applying a third voltage to the gate electrode, wherein the potential differences between the third voltage and the first and second voltages are sufficient to generate electric fields between the gate electrode and the source and drain regions to inject holes into the source and drain regions, respectively; and

switching the first voltage to the drain region and the second voltage to the source region at least one time during the predetermined erase time.

15. The method of claim 14, further comprising the step of applying a fourth voltage to the bulk region, the fourth voltage being less than or equal to the third voltage.

16. The method of claim 14, wherein time for switching between the first voltage and the second voltage is variable in the predetermined erase time.